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SCIENTIFIC DATA SYSTEMS

SDS 910/920-Input/Output

SDS 910/920 COMPUTERS
INPUT/OUTPUT

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PREFACE

This publication describes input/output operations of SDS 910/920 Computers. These machines have identical input/output systems. To better understand the following text, the reader should be familiar with the contents of SDS 910 or 920 Reference Manuals (SDS 900008 or SDS 900009).

Included in this book are descriptions of various types of input/output, interface information, considerations relating to grounding and an optional system to prevent loss of information during power failures.

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FIGURES

TABLES

TYPES OF INPUT/OUTPUT

The SDS 910/920 Computers use a wide variety of input/output systems for processing characters, words, and single-bit information.

BUFFER INPUT/OUTPUT SYSTEM

The central element of this standard input/output system is the W Buffer which consists of:

- 24-bit word assembly register
- Six-bit character register
- Six-bit unit address register
- Parity bit and associated circuitry
- Error flip-flop
- Input/output identifier flip-flop
- Two-bit character counter
- Two-bit character count register

An input/output operation is started by executing ENERGIZE OUTPUT M (02). The address portion of this instruction performs a number of functions: six bits identify the external device, connect this device to the buffer, and, if appropriate, start the device. One bit of these six sets the buffer to input or output mode. Two bits establish the number of characters per word. In addition to establishing these various conditions, ENERGIZE OUTPUT M (02) also copies the number of characters per word into the number-of-characters-per-word-counter, clears the error switch, and clears the character register. As soon as the first character arrives, it is stored in the 6-bit character register. In addition, a signal is sent from the data source to the buffer, indicating that the character register is loaded. With the arrival of this signal, which closes the input data loop, the character register is connected serially to the word register and a 24-bit circular left shift takes place through the word register. This process transfers the contents of the character register into the least significant bits of the word register. When the character is transferred to the character register, a seventh parity bit is checked by the buffer. If a parity error occurs, the parity bit is set and the control panel ERROR indicator is lit. Note that such an error does not stop the computer. Facilities are provided in the computer which allow the program to interrogate and reset this bit at a later time.

As soon as the contents of the character register have been shifted into the word register, the contents of the number-of-characters-per-word counter are decremented by one. If the new contents of this counter are still greater than zero, the buffer will wait for the next character. When the next character arrives the character register and the word register repeat the shifting operation described above. The information which was in the six right-hand bit positions of the word assembly register will be shifted left six bits, and the new contents of the character register will be shifted into the six right-hand positions of the word assembly register. When the character counter reaches zero, it initiates an interrupt to the computer, which forces the computer into a subroutine to handle the information stored in the buffer word register. Information is stored in selected sequential memory locations by a subroutine similar to the following:

Location	Instruction	Remarks
00031	BRM SUB	The interrupt causes this instruction to be executed.
SUB	(Return Address)	This is set by the instruction in location 00031.
	WIM LOC, 2	Transfer the contents of the buffer word register to the memory location specified by the address field (LOC) plus the contents of the index register.
	BRX $ +2	Add one to the index register. If the index register is still negative, skip the next instruction. If it is positive, take the next instruction in sequence.
	EOM 00000	Next instruction after entire block or record is loaded. The input operation is stopped and the buffer is disconnected.
	BRU *SUB	The exit from the subroutine. It branches to the stored return address and clears the interrupt channel.

While entering the block of information, the instructions in locations 31, SUB+1, SUB+2, and SUB+4 only are executed. The entire execution, including in-and-out linkage, requires 64 microseconds. An alternate method uses punched paper tape and magnetic tape. Here, a gap on the tape generates a second interrupt which signifies the end of a block. The program is as follows.

Location	Instruction	Remarks
00031	BRM SUB	When the buffer word register is filled, one interrupt causes this instruction to be executed.
00033	BRM PROG	When gap is encountered, the second interrupt causes this instruction to be executed.
SUB	(Return Address)	This is set by the instruction in location 00031.
	WIM LOC	The contents of the buffer are transferred to the memory location (LOC) specified by the address of the instruction.
	MIN SUB+1	The address portion of the WIM instruction is incremented by one.
	BRU *SUB	Control is returned to the main program of the location marked in SUB. The interrupt is reset.
PROG	(Retum Address)	This is set by the instruction in location 00033.
	EOM 00000	The buffer is cleared and readied for another I/O operation.
	BRU *PROG	Control is returned to the main program.

Note that none of the arithmetic registers were disturbed by the input subroutine. During the input process the main program can ascertain when the transfer of information is complete by testing the status of the buffer. If the buffer is ready, the transfer is complete and another I/O operation may be initiated.

The Buffer Interrupt System outputs data in a similar manner to input. Parity here is generated rather than checked. As noted above, a closed-loop synchronizing system is exercised to assure that no data is lost. During input this takes the form of a signal from the source indicating that data has been sent to the character buffer. During output, a signal from the destination of the data is used to time the loading of each character into the character register.

Data can be lost in one of two ways. During input, the word assembly register and the character register can both be full (if the program is not correct) at the time that another character is ready to be entered. If, for example, the source of data is a magnetic tape unit, information cannot be delayed and will be lost. Similarly, during output, if data has not been loaded into the word assembly register by the time it is demanded by the unit, a position on the magnetic tape will be empty. The computer always detects the occurrence of the error, stores the data in the I/O parity bit, sets the ERROR signal, and turns on the ERROR light.

The W Buffer can operate up to a maximum frequency of 62,500 characters per second under computer control.

BUFFER INTERLACE SYSTEM

This optional equipment makes use of the previously described W Buffer and, additionally, a 26-bit interlace register. This register is divided into two parts, a 12-bit counter and a 14-bit address. The register is loaded from the computer's memory by execution of PARALLEL OUTPUT (13), 24-bits, which loads the 14-bit address, ten bits of the counter, and sets the two most significant bits of the counter to zero. These two bits are provided to permit the counter to reach 4095. If these bits are required, they are set by ENERGIZE OUTPUT M (02) instructions. An entire block of information may now be copied into or read out of memory without interfering with other activities of the computer. The counter holds the number of words in a block. The address portion contains the initial address into which information is to be placed, or from which information is to be obtained. Because of the 14-bits, the address portion permits access to any memory location.

As with the Buffer Input/Output System, ENERGIZE OUTPUT M (02) initiates the input/output operation. Information flows, one character at a time, into the character register: the characters are shifted into the word assembly register; the character counter is decremented each time a new character is entered; and parity errors are sensed. When the character counter reaches zero an interrupt is <u>not</u> initiated. Instead, a number of other events occur. At the end of the memory cycle during which the buffer's character counter has reached zero, the computer is halted. The contents of the word assembly register are stored in the memory location specified by the present contents of the address portion of the interlace register. After this is accomplished, the computer is started again, the address part of the interlace register is incremented by one, and the counter is reduced by one. All of these operations require 16 microseconds during which time the buffer's character register can be accepting new information for the next word.

When the next word has been assembled, the character counter will have again gone to zero. The new word will be stored in the new address specified by the address portion of the interlace register: this procedure will continue until the interlace register's counter reaches zero. At this time an interrupt will occur and the computer will execute a program which acknowledges receipt of an entire block of information of up to 4095 words.

The system outputs data in a manner analogous to input and, similarly, requires 16 microseconds per word.

PRIORITY INTERRUPT SYSTEM

Each computer has two interrupt channels (30 and 31) as standard equipment, and two additional channels (32 and 33) if a Y Buffer is used. In addition, each computer may have as many as 896 channels of interrupt as optional equipment. These are supplied in groups of two. Two flip-flops are associated with each interrupt channel. These flip-flops indicate the status of the interrupt channel as follows:

FF1	FF2	Status
0	0	No interrupt received (Inactive)
1	0	Interrupt received but not being processed (Waiting)
1	1	Interrupt received and being processed (Active)
0	1	This is an unallowable configuration

The waiting condition exists if the computer is processing a higher priority interrupt, or if the computer is executing a long-duration operation, such as a shift or division, when the interrupt arrives; or if the interrupt system is in the disabled condition as a result of a program or control console switch setting. Always, the waiting status is maintained until it can be processed. For example, if the interrupt system had been in a disabled condition during the time when one or more interrupts occurred, and subsequently the interrupt system is enabled, each of the above-mentioned interrupts is processed in accordance with the priority system (described below). If an event occurs which produces a transitory signal on a given interrupt channel, such that the signal disappears prior to the time when the computer can process it, the waiting status is maintained continuously until processed.

If a higher priority interrupt occurs during the time when an interrupt on a given channel is being processed, the given interrupt channel remains in the active status, but the program will transfer to the location associated with the higher priority interrupt. After processing this interrupt, the program returns to the initial interrupt and from there to an intermediate priority interrupt if one is waiting. While in the active status, the interrupt channel rejects new signals. Consequently, if an interrupt signal is presented to a given interrupt channel while the computer is processing an interrupt on that given channel, the computer will ignore the signal regardless of its duration or the number of times it has occurred, until the active status has been terminated by the execution of an appropriate instruction (described below). A safety system is built into the "power-on" sequencing system such that all interrupt channels are set to the inactive status when computer power is turned on and the START switch is pressed. This prevents random conditions which might otherwise occur during "power-on" cycling. Such random conditions could force the computer to process interrupts of events which did not occur.

The interrupt system can be disabled by executing the appropriate ENERGIZE OUTPUT M (02); however, the interrupts associated with the power safety system cannot be disabled.

An interrupt occurring on a given interrupt channel causes the computer to execute the instruction in a memory location which is unique to the given channel. This unique location contains the next instruction to be executed, usually a MARK PLACE AND BRANCH (43). For example, if the computer is executing an instruction from memory location 0500 at the time when an interrupt signal occurs on channel 32, the computer completes the execution of the current instruction, and takes its next instruction from memory location 32. If the interrupt occurred on channel 0673, the computer would take its next instruction from memory location 0673. This transfer does not alter the program counter. Therefore, although the interrupt instruction being executed is in location 32 or 0673 in this example, the program counter contains the number 0501, the location of what would normally be the next instruction. Here the interrupt acts like an EXECUTE instruction.

Because each interrupt forces the computer to execute the contents of a location which is unique to the interrupting channel, it is not necessary to provide a time and memory space-consuming subroutine which looks back to determine the cause of the interrupt. If the computer executes the instruction stored in N, it is because a particular event occurred.

Processing of a normal interrupt always requires the execution of more than one instruction. The interrupt location must contain MARK PLACE AND BRANCH (43), which provides entry to an appropriate subroutine, preserving the return address in the subroutine. The following short program is an example that assumes an interrupt on channel 205:

Location	Instruction	Remarks
01522	ADD A	Instruction being executed when interrupt occurred.
00205	BRM INT	The interrupt forces this instruction to be executed. The address 01523 is stored in location INT and control branches to INT+1.

Location	Instruction	Remarks
INT	PZE 01523	Return address. The address of the instruction following ADD A is stored in this location.
.	.	Interrupt subroutine.
.	.	
.	.	
	BRU *INT	Last instruction of subroutine. This instruction with indirect address tells the computer to transfer control to the location containing the return address and clears the interrupt channel.
01523	STA B	Next instruction to be executed in main program after the interrupt.

The BRU *INT instruction changes the status of the highest priority currently active interrupt channel to inactive.

Each interrupt channel has its own unique priority and the priority order is inversely related to interrupt channel identification numbering. Thus, the channel with the highest number has the lowest priority, and the channel with the lowest number has the highest priority.

THE Y BUFFER

A second buffer, the Y Buffer, which is available as an option, is identical to the W Buffer system in all respects except that the character register can contain from 6 to 24 bits. This feature permits the computer to translate one magnetic tape format—such as IBM format—into a format that uses a different character length. The Y Buffer can operate with or without interlace at a frequency of up to a maximum of 62,500 characters per second under computer control. If the character buffer is 24 bits, then each character can be externally broken into four 6-bit characters to obtain a maximum frequency of 250,000 six-bit characters per second.

WORD PARALLEL SYSTEM

Two standard instructions, PARALLEL OUTPUT (13) and PARALLEL INPUT (33), permit any word in the memory to be presented, in parallel, at a connector; or, inversely, permit signals to be stored in any memory location. The execution of either PARALLEL INPUT (33) or PARALLEL OUTPUT (13) provides a signal to the external device that signifies the computer is ready for the transmission of data. During input the computer will lock-up in PARALLEL INPUT (33) until the selected external device has presented its information, together with a ready signal. Only after the computer has detected this ready signal can it terminate PARALLEL INPUT (33) and proceed with the program. As in the W Buffer System, all transmissions are close-looped. To overcome the possibility of lock-up, the ready signal from the external device can be used to initiate an interrupt to the computer which will cause the computer to jump to PARALLEL INPUT (33). Thus, the computer is free to execute other programs except during the time when it must accept and store information appearing at the parallel input connector.

If PARALLEL INPUT (33) is to be used to store a series of data words in numerically sequential memory locations, some means must be found for modifying its address. This can be accomplished in a number of ways; an indexed PARALLEL INPUT (33) instruction is one such way. A subroutine consisting of an indexed PARALLEL INPUT (33) followed by INCREMENT INDEX AND BRANCH (41) can be used and requires 40 microseconds. Approximately 25,000 words per second can be entered in this mode. The parallel output operation is similar to the parallel input operation except that the timing is 32 microseconds. The computer will lock-up in PARALLEL OUTPUT (13) until it receives a signal from the selected device, indicating that it can receive information. The interrupt can be used to overcome this possible difficulty as previously described. The "locking" feature of PARALLEL INPUT (33) is most useful when a high input rate must be obtained and simultaneous computation is not required. The computer is thus slaved to the clock of the sending device. The ready signal from the external device is used to initiate an interrupt when simultaneous computation provides a system advantage. When interrupt is used, a total of 32 microseconds is added to the program time for each word transferred.

PARALLEL INTERLACE SYSTEM

This optional system has an interlace register to control parallel inputs or outputs with a single PARALLEL INPUT (33) or PARALLEL OUTPUT (13). To initiate an input operation, appropriate instructions are used to load the interlace register with the first address into which the information is to flow, and with the number of words to be entered.

When PARALLEL INPUT (33) is executed, the previously selected device will present its contents to the Pin connector, and from there it will be stored in the memory location specified by the address contained in the interlace register. The address portion of PARALLEL INPUT (33) is not used in the interlace mode. When the contents of the selected input device have been transferred to the location specified by the address in the interlace register, this register is automatically modified (that is,

the address and counter will be incremented by one). Also, a synchronizing signal is sent to the input device indicating that the computer is ready for the next input. This procedure of entering information, modifying the interlace register, and notifying the input device, will continue until the counter of the interlace register reaches zero. At this time, PARALLEL INPUT (33) is terminated and the computer obtains its next instruction from the next sequential location. Transfers are asynchronous at a maximum rate of 8 microseconds per word.

Output operates in a similar manner. The interlace register in the Parallel Interlace System can also be used with either the W or Y Buffers. Only two interlace registers can be put in action with any computer.

ACTUATE AND TEST EXTERNAL DEVICE SYSTEM

This system uses the two instructions, ENERGIZE OUTPUT M (02) and SKIP IF SIGNAL NOT SET (40). When ENERGIZE OUTPUT M (02) is executed, the computer sends a configuration of ones and zeros, corresponding to the bits of the address portion of the instruction, to the Eom connector pins. These signals are zero volts for binary zeros, and plus eight volts for binary ones. The instruction lasts for eight microseconds and presents its address signals to connector pins for eight microseconds. Certain address configurations have been reserved to perform specified operations. These are described in Appendix D of SDS 910/920 Reference Manuals.

The address bits of SKIP IF SIGNAL NOT SET (40) are used to address an external device. If the addressed device is presenting a plus eight-volt signal to the computer at the time when SKIP IF SIGNAL NOT SET (40) is being executed, the computer will take its next instruction from the next sequential location. If the addressed device is presenting a zero volt signal at this time, the computer will skip the instruction in the next sequential location and execute the following one next. Special configurations of address bits are reserved for testing certain devices and conditions. These are described in Appendix D of SDS 910/920 Reference Manuals.

SPECIAL PRIORITY INTERRUPT SYSTEM

This system differs from the normal Interrupt System in that the location to which the program is forced cannot contain a branch instruction. The system is based on use of subroutines consisting of a single instruction. These single-instruction subroutines are located in the forced locations. In this system the execution of the instruction located in the forced location terminates the active status of the interrupt, returning it to the inactive status. The program counter is not altered by execution of the interrupt, and consequently the computer will obtain its next instruction from the location immediately following the one being executed when the interrupt occurred. This system of interrupts can be applied to a variety of uses, such as the tallying of the occurrences of a given event, or the counting of time pulses. As each event occurs, it causes a special interrupt channel to be activated, causing the computer to execute MEMORY INCREMENT (61). The execution of this instruction adds one to the contents of the memory location being used as a counter for this event, and the main program is automatically continued. Any number of counters (up to 896) can be used. The signal activating the interrupt must be of a duration greater than eight microseconds but less than 16 microseconds. Maximum repetition frequency is determined by the execution time of the longest instruction in the main program and by the execution time of higher priority subroutines.

In an alternate use, when an external device is ready to present parallel information to the computer, it can activate a special interrupt which will cause the computer to execute PARALLEL INPUT (33), previously described. Following execution of this instruction the computer will return to the main program and continue operation.

Any or all channels of a priority interrupt group can operate as special interrupts. The instruction located in the forced location must be of a type that takes more than one cycle to execute.

PRECEDENCE OF INPUT/OUTPUT FUNCTIONS

Various input/output systems can operate simultaneously; therefore, it is important to establish the ordering of various functions.

1. Interlace operations have the highest precedence and occur at the start of the next computer cycle. If two Interlace Registers are used, Y has precedence over W.

2. Interrupt operations have the next highest precedence but are not initiated until the end of the current instruction. Two interrupts associated with the power system—if they are used—have the highest priority; then those associated with the Y and W Buffers; then the remaining channels.

INTERFACE CONNECTIONS

INTRODUCTION

This section describes the basic logic connections and electrical characteristics of the input/output system together with timing and logic diagrams

INTERFACE CIRCUITS AND CABLE REQUIREMENTS

SIGNAL CHARACTERISTICS

All input and output signals are dc levels with the following characteristics and requirements:

DC Signal Levels

Voltage levels of logical "one" and "zero" are respectively +8 and zero.

Output Logic Levels

One (true)	+9.5 to +6.5v
Zero (false)	+0.6 to 0v

Input Logic Levels

One (true)	+20.0 to +5v
Zero (false)	+2.0 to -2.0v

Unit Load

A unit load is defined as 3ma to the driving source at the 0v level, and no current at the +8v level.

Because the same logic term may appear on several input/output connectors, the allowable load currents given must be shared between all input/output connectors.

Output Signal Characteristic

Source impedance	820Ω to +8.0v

Input Signal Characteristics

Input impedance	2.7k to +25v
Rise time	The timing diagrams show the specific time at which the dc input signal must be at a "true" level (+20 to +5v)
Fall time	The timing diagrams show the specific time at which the dc input signal must be at a "false" level (+2.0 to -2.0v).

Connectors

All connectors are 47-pin ELCO Varicons.

CABLE CONSIDERATIONS

Cables whose wires are individually shielded should always be used. The preferred cables are specified in SDS Drawings:

101787	14- Conductor (Individually Shielded) Cable
102872	30-Conductor (Individually Shielded) Cable

These cables have the following approximate characteristics:

Inductance	50μh/ft
Capacitance	50pf/ft
Characteristic Impedance	33 Ω
Resistance of Center Conductor	23mΩ/ft
Resistance of Shield	10mΩ/ft

CIRCUIT CONSIDERATIONS

All output drive circuits from the 910/920 Computers are transistor switches to ground. The three most important circuit considerations relating to cabling are:

-noise in the cable

-loading of the drive source

-signal delay

Careful consideration of these three points must be given in any application.

A recommended drive network is shown in Figure 1, and a table of values for R and L is presented in Table 1. The output capability of the SDS 910/920 drive circuit is 26 unit loads. These drive circuits are shared by the tape unit, Y Buffer, and memory interlaces.

Table 2 lists the equivalent unit loading for each of these equipments. If the equipment configuration exceeds 26 unit loads, it is necessary to add a Model 9126 Signal Coupler (refer to SDS Technical Manual 900861). Count two unit loads for the 9126 Signal Coupler.

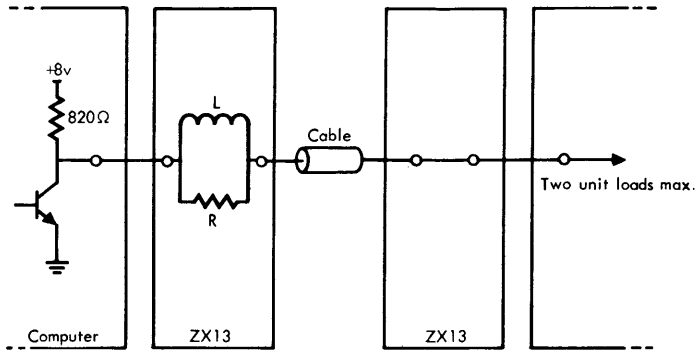


Figure 1. Drive Network

Table 1. Values for R and L

Cable Length (feet)	T_D (μsec)	R (Ω)	L (μh)	N
5	0.24	470	220	8
10	0.35	390	220	9
20	0.47	330	220	10
30	0.57	270	220	12

T_D = signal delay

N = effective unit loads

Table 2. Equivalent Unit Loading

Equipment	Unit Loads
Magnetic Tape Unit	10
Y Buffer	4
Memory Interlace	5 each

Signals driven back to the computer should have similar drive networks. In addition, these signals should be decoupled to prevent interaction between other devices and to isolate remote equipment if the remote power is off. The recommended connection is shown in Figure 2.

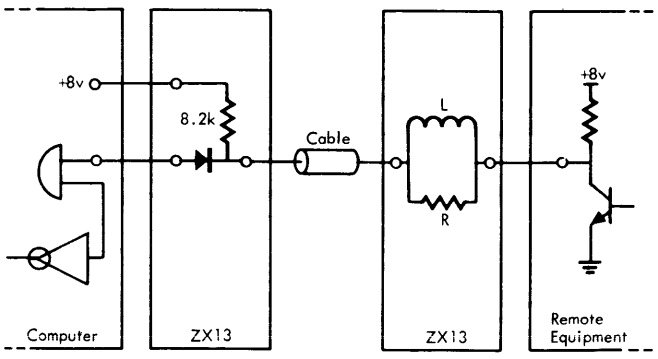


Figure 2. Recommended Decoupling Connection

The Interrupt Input Network differs from all others. A recommended drive configuration is shown in Figure 3. All interrupts which are not used will continuously interrupt the computer. Therefore, it is recommended that unused interrupt channels be grounded.

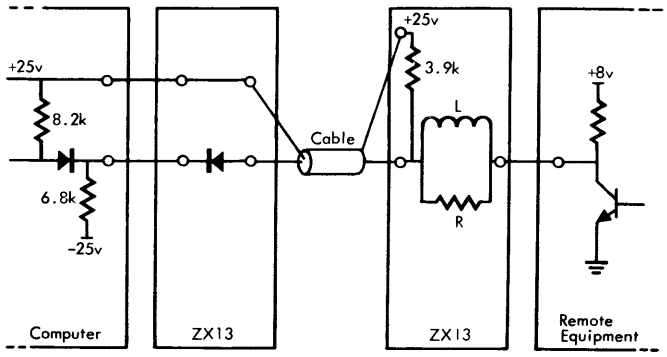


Figure 3. Recommended Drive Configuration

PARALLEL OUTPUT/ENERGIZE M CONNECTORS

Connector locations 4G and 5G are supplied with the same signals and have two major functions.

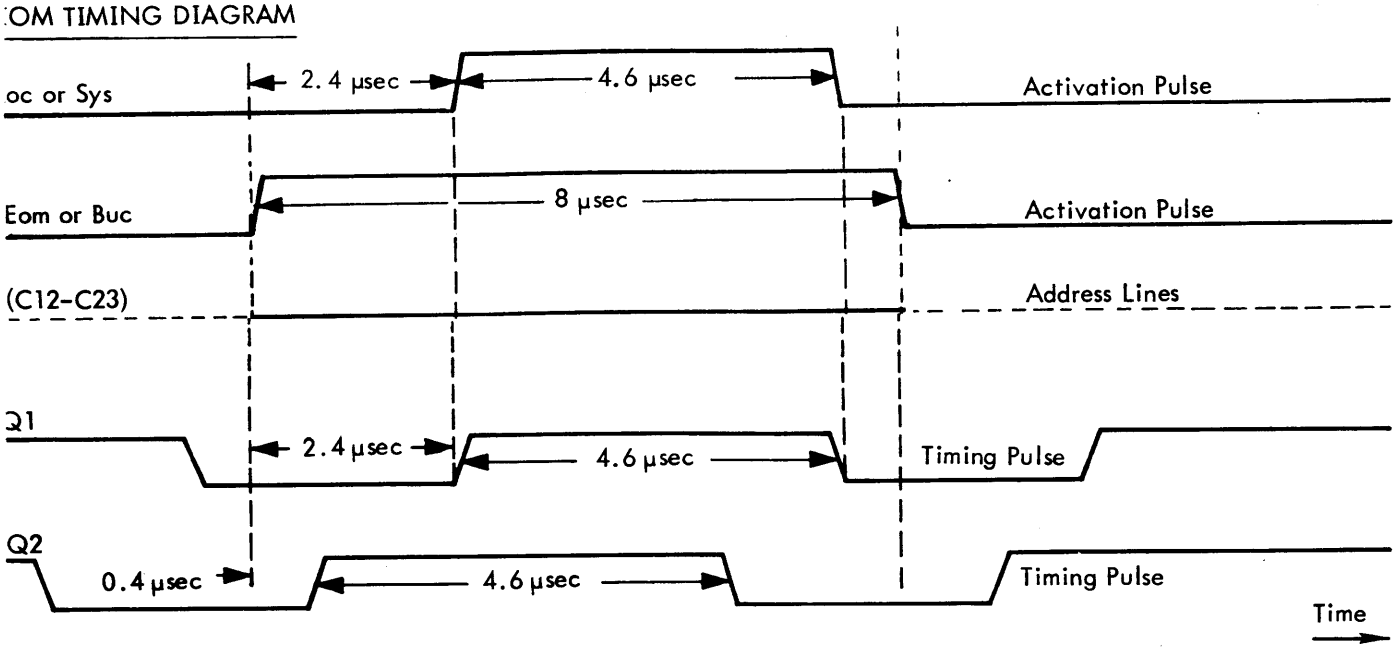
1. When using the ENERGIZE OUTPUT M (EOM) instruction: During execution of instruction 02 (EOM) an eight-microsecond activation pulse is sent out on the Eom line. Depending on "C" register bits C9, C10, and C11, one of three other lines may carry a pulse. C1 and the 12 bits of the effective address must be decoded by the external device to determine if EOM is for this device.

For EOM's with $\overline{C9}$, C10, C11, a 4.6 microsecond Sys pulse is generated. For EOMs with $\overline{C10}$, C11, a 4.6 microsecond Ioc pulse is generated. For EOMs with $\overline{C10}$, $\overline{C11}$, an eight microsecond Buc pulse is generated. All other EOM configurations must use Eom pulse and external gating. The 12 address lines are designated C12 through C23. Decoding of the address lines and gating of the activation signal must be accomplished externally.

2. When using the PARALLEL OUTPUT (POT) instruction: The contents of the effective address are held in the C register for parallel transfer to an external device which has been previously addressed by ENERGIZE OUTPUT M (02). Unless the external device is currently in a READY state, the computer will lock-up until released by the external device.

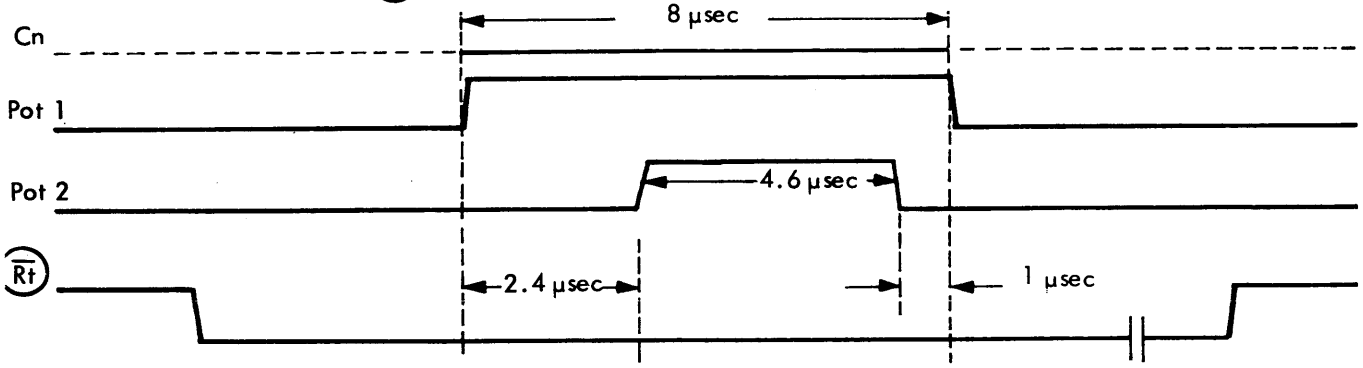
The 24 parallel output lines from the C register are designated C0 through C23, with C0 as the most significant bit. Since the information on the C register outputs is changing during other operations, STROBE signals designated Pot 1 and Pot 2 are provided. A READY signal designated $\overline{Rt}$ (Inverse Logic) must be provided by the external device to release the computer.

:OM TIMING DIAGRAM

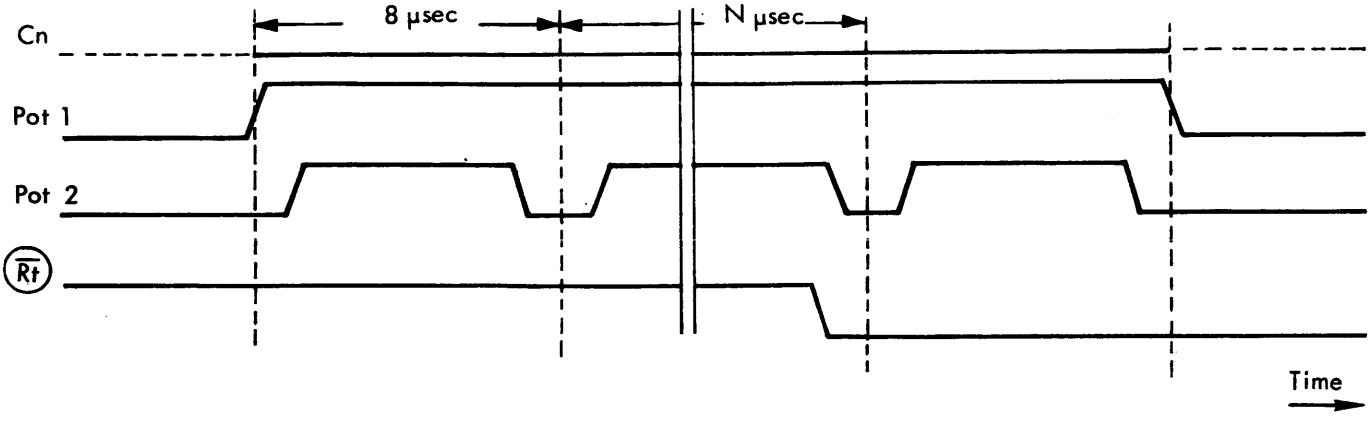


Note: The C12 through C23 output lines are changing or are at undefined levels, except during the eight microseconds when Ioc or Sys is true.

POT TIMING DIAGRAM A: $\overline{Rt}$ = Ready before computer reaches output phase



POT TIMING DIAGRAM B: $\overline{Rt}$ = Ready after computer reaches output phase



CONNECTORS

The parallel output connector position is 4G. Position 5G is supplied with the same signals but is normally used for ENERGIZE OUTPUT M (02). To connect external cables to position 4G or 5G, use SDS Cable Plug ZX13. The cable length from position 4G or 5G to the rear of the computer is two feet.

Pin	Term	Function
1	Pot 1	An output signal which signifies that the computer is in the parallel output phase, and that the C register outputs are ready. MAXIMUM LOAD from 25 ma to positive voltage (+v) MINIMUM SIGNAL DURATION 8μsec
2	Pot 2	An output signal derived from Pot 1 which is used to STROBE the C outputs. MAXIMUM LOAD 50 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
3	Ioc	The EOM activation signal generated for controlling computer input/output equipment. The "Ioc" signal must be gated externally with the address lines to determine its destination. MAXIMUM LOAD 150 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
4	Buc	An EOM signal generally used with W and Y Buffers. MAXIMUM LOAD 50 ma to +v MINIMUM SIGNAL DURATION 8 μsec
5	Sys	The EOM activation signal generated for controlling systems equipment and undefined external devices. The SYS signal must be gated externally with the address lines to determine its destination. MAXIMUM LOAD 150 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
6	Eom	The EOM signal that is always present independent of the type of equipment addressed. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION 8 μsec
7	Q1	A computer generated timing signal. May be used for external timing/gating. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
8	Q2	A computer generated timing signal. May be used for external timing/gating. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
9	Pin	Designates to the external device the period during which the computer is strobing the input lines. See Parallel Input Connector. MAXIMUM LOAD 50 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
10	$\overline{\text{Rti}}$	Designates that the Pin phase is complete. See Parallel Input Connector. MAXIMUM LOAD 50 ma to +v MINIMUM SIGNAL DURATION 8 μsec
12	(Mtg)	An input signal from magnetic tape stations identifying the gap condition
14	($\overline{\text{Sio}}$)	An input signal used to sense various external conditions. This signal is normally used in

Pin	Term	Function
14 (Cont)		conjunction with computer input/output equipment such as testing the the status of Mag. Tape #5, Typewriter #2, etc. See SKIP ON EXTERNAL SIGNAL connectors. MINIMUM SIGNAL DURATION Depends upon the program.
15	(Ssc)	An input signal used to sense various external conditions. This signal is normally used in conjunction with external systems and undefined external devices. See SKIP ON EXTERNAL SIGNAL connectors. MINIMUM SIGNAL DURATION Depends on the program.
16	(Rt)	This is the READY signal supplied by the external device, and indicates that the external unit is ready to receive the parallel output data. The output will continue for one word time after the external device is ready. This signal must be at zero volts for a minimum of 8 μsec and must be at zero volts immediately before or during Pot 1.
17	St	An internal computer reset signal generated by the START switch. It can be used to reset external devices at the start of operation. MAXIMUM LOAD 100 ma to +v MINIMUM SIGNAL DURATION Manual operation
18	$\overline{C17}$	See W Buffer input/output connectors. This term used to specify W Buffer operations where C17 is used to specify Y Buffer operations.
20 thru 43	C0 thru C23	These output signals represent the contents of the 24-bit data word, with C0 representing the most significant bit. The signals on these outputs will be changing or will be in an undefined state except for the period when Pot 1 or EOM is true. Positive logic is used on the data signals. C12 through C23 are the effective address lines used with the EOM command. They designate which external device is to receive the activation pulse. These signals are decoded and gated externally with the activation pulse. MAXIMUM LOAD 10 ma to +v MINIMUM SIGNAL DURATION 8 μsec

PARALLEL INPUT CONNECTOR

The computer "locks-up" in an input phase and samples information (up to 24 parallel bits) from the external device until it is released by the external device. It will then adjust parity and store the data word in a memory location designated by the effective address.

The 24 parallel input signals from the external device are designated ($\overline{Cd0}$) through (Cd23), with ($\overline{Cd0}$) representing the most significat bit. A READY FOR INPUT signal, designated Pin, is generated by the computer. An additional READY ($\overline{Rt}$) signal is required from the external device to release the computer.

CONNECTORS

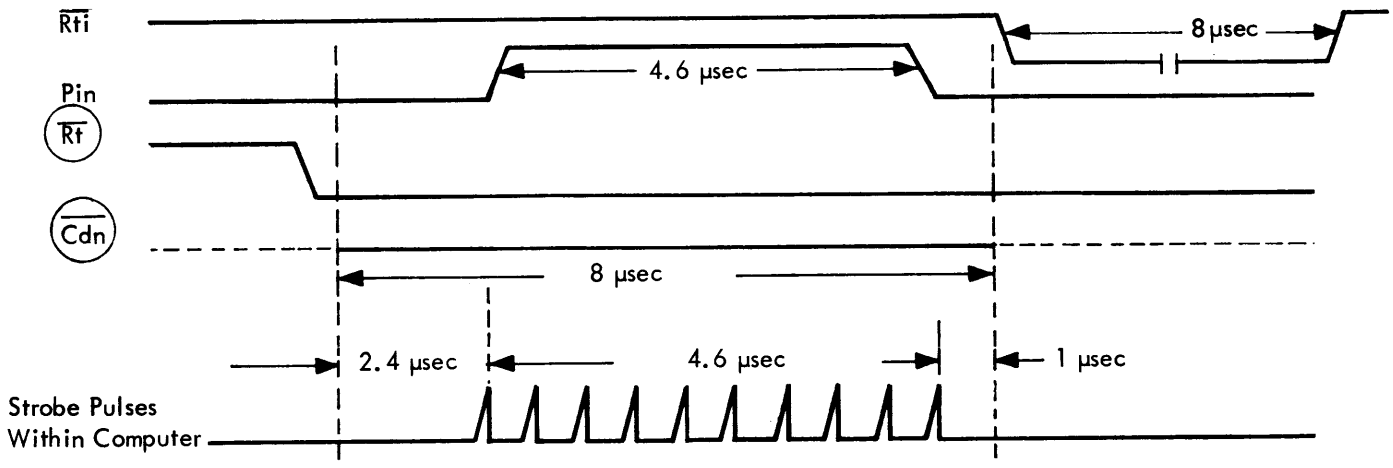
The parallel input connector is designated 12G. To connect external cables to position 12G, use SDS Cable Plug ZX13. Cable length from position 12G to the back of the computer is 2.5 feet.

Pin	Term	Function
1	Pin	Designates to the external device the period during which the computer is strobing the input lines. MAXIMUM LOAD 50 ma to +v SIGNAL DURATION 4.6 μsec
3	($\overline{Sio}$)	An input signal used to sense various external conditions. This signal is normally used in conjunction with computer input/output equipment such as testing the status of Mag. Tape #5, Typewriter #2, etc. (see LOGIC DIAGRAM A).

Pin	Term	Function
		MINIMUM SIGNAL DURATION Depends upon the program.
8	$\overline{Rti}$	Designates that the Pin phase is complete. MAXIMUM LOAD 50 ma to +v SIGNAL DURATION 8 μsec
16	$\overline{Rt}$	This is the READY signal supplied by the external device, and indicates the external unit is ready to enter data on the parallel input lines. The strobing of the input lines will not occur until after the READY signal is at zero volts.

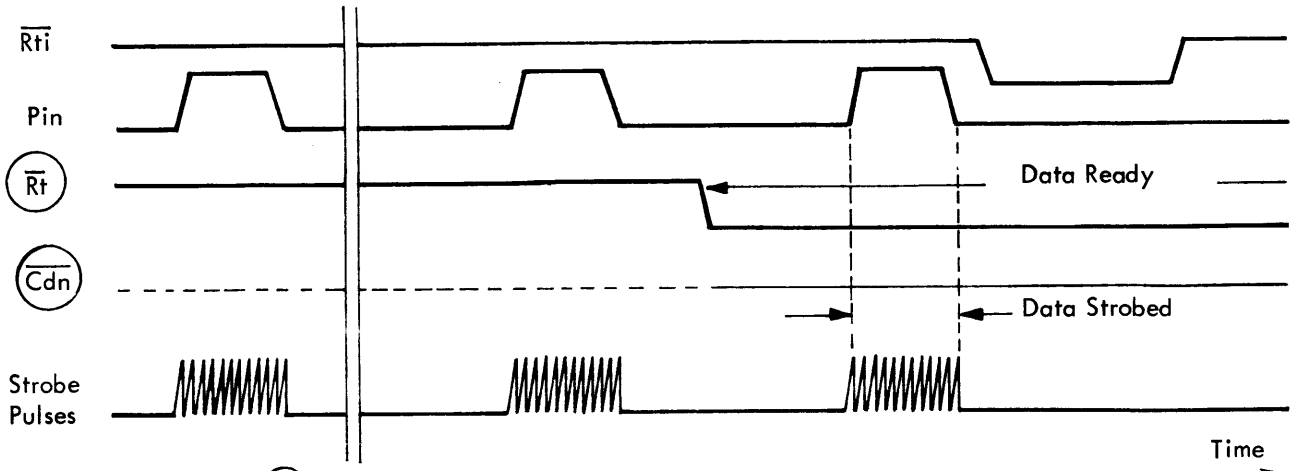
Pin	Term	Function
		MINIMUM SIGNAL DURATION 8 μsec
20 thru 43	$\overline{Cd0}$ thru $\overline{Cd23}$	These signals represent the 24 parallel input lines to the computer. Note that the logic is inverted and a ONE on the input line is represented by a level of zero volts. These signals may be changing or be in an undefined condition until $\overline{Rt}$. They must be stable during the Pin strobe time. The Pin strobe may be used for pulsing in a transformer-coupled system.

TIMING DIAGRAM A



$\overline{Rt}$ = Ready Before Computer Reaches Input Phase

TIMING DIAGRAM B



$\overline{Rt}$ = Ready After Computer Reaches Input Phase

W BUFFER INPUT/OUTPUT CONNECTORS

External devices communicating with the computer through the W Buffer can be connected to one of four identical auxiliary equipment connectors. See the Reference Manual for details on buffer operation and external equipment addressing.

Six channels of information can be accepted by the buffer through the input lines designated (Zw1) through (Zw6). The six output lines from the buffer are designated R1 through R6. Buffer unit address terms and input/output unit control address terms are also provided as well as strobing and sync terms.

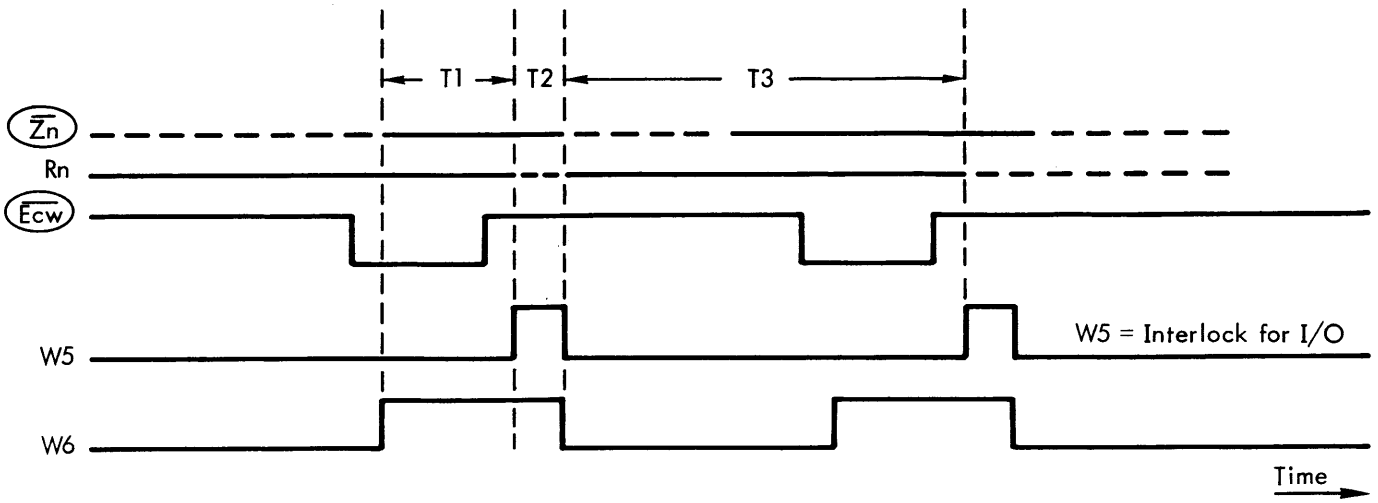
CONNECTORS

Four separate but identical connector positions are supplied for the W Buffer Auxiliary Input. These positions are 7G, 8G, 9G, and 10G. To connect external cables to positions 7G, 8G, 9G, or 10G, use SDS Cable Plug ZX13. The cable length from positions 7G, 8G, 9G, or 10G, to the rear of the computer is 2.5 feet.

Pin	Term	Function
1 thru 6	(Zw1) thru (Zw6)	A character of up to six bits in length can be fed to the W Buffer on lines (Zw1) through (Zw6). Note that the logic levels are inverted and a ONE on an input line will be represented by zero volts. Zw6 becomes the least significant bit in the accumulated word. MINIMUM SIGNAL DURATION The input signals must be stable during and 8 μsec beyond the (Ecw) clock time.
7	(Zwp)	Seventh channel ODD parity input to W Buffer. MINIMUM SIGNAL DURATION The input signals must be stable during and 8 μsec beyond the (Ecw) clock time.
8	(Ecw)	Input or output clock supplied by the external device. Specific input rate depends upon program (zero volts true). MINIMUM SIGNAL DURATION 8 μsec
9	(Whs)	EXTERNAL HALT SIGNAL to W Buffer. MINIMUM SIGNAL DURATION Depends on program.
10	(Sio)	An input signal used to sense various external conditions. The signal is normally used in conjunction with computer input/output equipment such as testing the status of Magnetic Tape #5, Typewriter #2, etc. See SKIP ON EXTERNAL SIGNAL connectors. MINIMUM SIGNAL DURATION Depends on program.
11	BUC	An EOM signal generally used with W and Y Buffers. MAXIMUM LOAD 50 ma to +v MINIMUM SIGNAL DURATION 8 μsec
12	Np	An external signal which is held to zero volts when input parity (Zwp) will not be supplied.
13	(Wes)	An externally generated signal used to set the error condition in the W Buffer. MINIMUM SIGNAL DURATION 8 μsec (depends on program)
14	W0	An internal signal which states that the buffer has read two data characters. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION Depends upon length of process.
15	W5	A Flip-flop which states that the buffer is ready to receive a new clock. (Ready when W5 is at zero volts.) MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION 8 μsec

Pin	Term	Function
16	W6	A Flip-flop which states that the input clock or output clock has been detected. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION Length of clock plus 8 μsec
17	Q2	A clocking term supplied for clocking into external flip-flops (stage of pulse-time counter). MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION 3.8 μsec; FREQUENCY 125 kc
18	Ioc	The Eom activation signal generated for controlling computer input/output equipment. The "Ioc" signal must be gated externally with the address lines to determine its destination. MAXIMUM LOAD 150 ma to +v MINIMUM SIGNAL DURATION 4.6 μsec
19 thru 24	W9 thru W14	Peripheral unit address terms. See Reference Manual for additional buffer addressing information.
25 thru 30	R1 thru R6	The six output lines from the W Buffer representing a character. R6 represents the least significant bit of the character. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION The output is stable as long as W5 is false, or as long as $\overline{Ecw}$ is at zero volts.
31	Rp	The ODD parity bit generated by the W Buffer for each output character. MAXIMUM LOAD 25 ma to +v MINIMUM SIGNAL DURATION The output is stable as long as W5 is false, or as long as $\overline{Ecw}$ is at zero volts.
32 thru 43	C12 thru C23	Address portion of the C register. Pin 37 presents $\overline{C17}$ rather than C17 on W Buffer auxiliary connectors. (Y Buffer auxiliary connector is identical to W except pin 37 presents C17.)

TIMING DIAGRAM



T1 - Data read into character register by computer

T2 - Data transfer between character and word register

T3 - Data read out of character buffer by external device during $\overline{W5}$

SKIP ON EXTERNAL SIGNAL CONNECTORS

Instruction SKIP IF SIGNAL NOT SET (40) will cause the computer to skip from location L to location L +2 if the specified input line is not true. There are two Sks input lines designated for external use, $\overline{\text{Sio}}$ and $\overline{\text{Ssc}}$. Address bits C10 and C11 determine internally which of these, $\overline{\text{Sio}}$ or $\overline{\text{Ssc}}$, is to be tested. $\overline{\text{Sio}}$ is tested for $\overline{\text{C10}}$ C11 and $\overline{\text{Ssc}}$ is tested for C10 C11. Address bits C1 and C12 through C23 can be decoded externally to gate several signal lines into $\overline{\text{Sio}}$ or $\overline{\text{Ssc}}$. The address lines are held fixed for eight microseconds prior to the time the computer samples $\overline{\text{Sio}}$ or $\overline{\text{Ssc}}$.

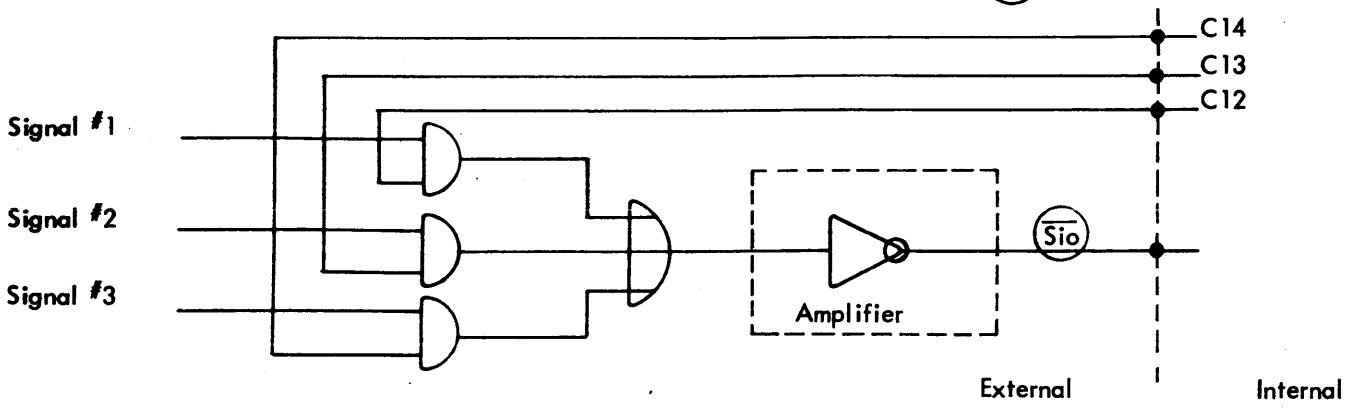
CONNECTORS

Input signal $\overline{\text{Sio}}$ appears on connectors 4G, 5G, 12G, 7G, 8G, 9G, and 10G, and input signal $\overline{\text{Ssc}}$ appears on connectors 4G and 5G. To connect external cables to the positions listed use SDS Cable Plug ZX13. The cable length from positions 4G through 12G to the rear of the computer is 2.5 feet.

Term	Connector and Pin	Function
$\overline{\text{Sio}}$	4G 14 5G 14 12G 3 7G 10 8G 10 9G 10	An input signal used to sense various external conditions. This signal is normally used in conjunction with computer input/output equipment
	10G 10	such as testing the status of Magnetic Tape #5, Typewriter #2, etc. (see LOGIC DIAGRAM A). MINIMUM SIGNAL DURATION Depends upon the program.
$\overline{\text{Ssc}}$	4G 15 5G15	An input signal used to sense various external conditions. This signal is normally used in conjunction with external systems and undefined external devices (see LOGIC DIAGRAM B). MINIMUM SIGNAL DURATION Depends upon the program.
C12 thru C23	4G 32 - 4G 43 5G 32 - 5G43 7G 32 - 7G 43 8G 32 - 8G 43 9G 32 - 9G 43 10G 32 - 10G 43	Address lines supplied for the decoding of several external conditions. On connectors 7G, 8G, 9G, and 10G, $\overline{\text{C17}}$ is supplied instead of C17. The output lines from the C Register are stable for 8 microseconds prior to the time that $\overline{\text{Sio}}$ or $\overline{\text{Ssc}}$ is tested. MAXIMUM LOAD 10 ma to +v

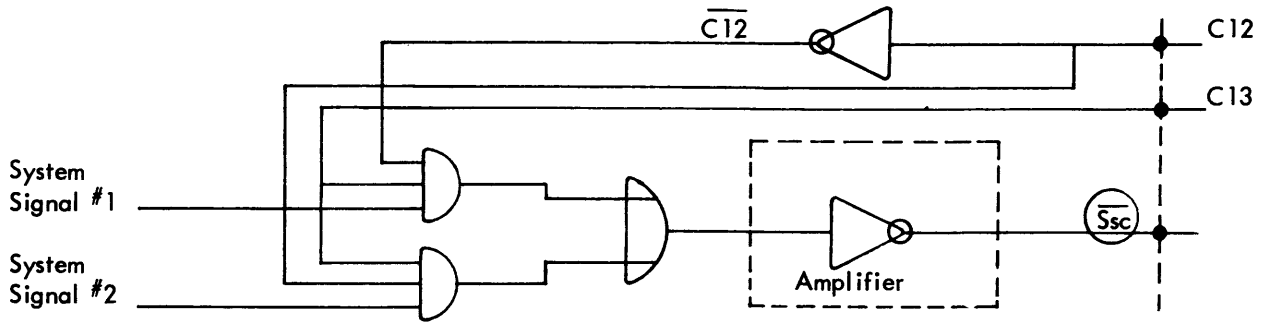
LOGIC DIAGRAM A

An example of EXTERNAL DECODING of several input lines to the $\overline{\text{Sio}}$ signal.



LOGIC DIAGRAM B

An example of EXTERNAL DECODING of several input lines to the $\overline{Ssc}$ signal.



Using C1 and C12 through C23 the decoding can be expanded to 2^{13} terms.

External Internal

CHANNEL INTERRUPT SYSTEM

Four channels of interrupt are built into each SDS 910/920 Computer but are used only for buffer operation. Additional interrupt channels can be purchased in groups of two. To convert to single instruction interrupt, see below:

CONNECTORS

All channels of interrupt connect to position 26 of Interrupt Chassis 9328/29. To connect external cables to Interrupt Chassis 9328/29, use SDS Cable Plug ZX13. The cable length from the interrupt unit to the rear of the computer is a maximum of four feet.

Pin	Term	Function
5 thru 20	I 5 thru I 20	When an external interrupt signal is held true for at least 8 microseconds, the computer will transfer to a specified address at the completion of execution of its present instruction (provided that an interrupt of higher priority is not present).

SIGNAL DURATION:

Minimum: 8 μsec

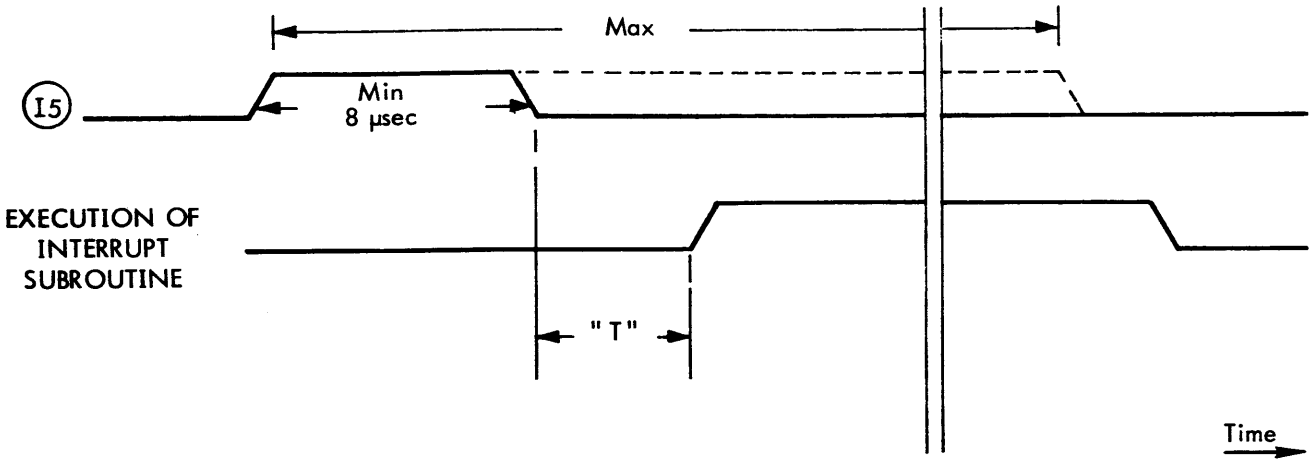
Maximum: 16 μsec for single execution interrupts. For other interrupts it must reset before the interrupt subroutine terminates.

SINGLE INSTRUCTION INTERRUPT

To convert any standard interrupt channel to a single execution interrupt channel a jumper must be added to the interrupt chassis.

Channel	Jumper
I 5	27-1 to 30-29
I 6	27-2 to 30-18
I 7	27-4 to 31-29
I 8	27-6 to 31-18
I 9	27-8 to 32-29
I 10	27-9 to 32-18
I 11	27-11 to 33-29
I 12	27-13 to 33-18
I 13	27-14 to 34-29
I 14	27-15 to 34-18
I 15	27-16 to 35-29
I 16	27-17 to 35-18
I 17	27-19 to 36-29
I 18	27-21 to 36-18
I 19	27-23 to 37-29
I 20	27-24 to 37-18

TIMING DIAGRAM



"T" DEPENDS UPON THE INSTRUCTION BEING EXECUTED AT THE TIME OF INTERRUPT OR EXECUTION TIME OF HIGHER PRIORITY INTERRUPTS WHICH ARE PRESENT.

GROUNDING FOR INPUT/OUTPUT

All SDS equipment is designed to avoid system grounding problems. Up to four separate grounds may be required in a system.

1. The analog ground associated with signal sources such as transducers.

2. The multiplexer - analog-to-digital converter ground. This is also normally the digital-to-analog ground.

3. The computer and other digital equipment ground.

4. The ac power ground.

These grounds are separated as follows:

1-2: by use of differential amplifiers.

2-3: by use of transformer coupling of all synchronizing and information signals (standard in SDS converters and multiplexers);

4: through power supply isolation.

POWER FAIL-SAFE SYSTEM

The SDS 910/920 Computers are designed to accept an optional power-sensing and interrupt system. Upon failure of the main power to the computer, the contents of all registers and other changeable information are automatically stored in the core memory and further writing into core storage is inhibited during the decay period of the computer dc power supply outputs.

The system consists of a relay-controlled ac power-sensing and memory-sequencing system, two priority interrupt channels, and a "shut-down/start-up" programming package.

In case of power loss, the computer is interrupted. The program is sent to location 037 (the linkage to a shut-down routine) which constructs an appropriate linkage at 036, such that computation can be immediately resumed when power is restored. At this time, the START signal is actuated to initialize the computer. An interrupt then sends the program to location 036, restarting computation.

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